UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
|---|---|---|---|---|
| 10/623,916 | 07/21/2003 | Gerd K. Binnig | CH920000082US1 | 5369 |

36380 7590 10/03/2005

RICHARD M. GOLDMAN
371 ELAN VILLAGE LANE
SUITE 208, CA 95134

| EXAMINER | |
|---|---|
| FLOURNOY, HORACE L | |

| ART UNIT | PAPER NUMBER |
|---|---|
| 2189 | |

DATE MAILED: 10/03/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 10/623,916 | BINNIG ET AL. | |
| | Examiner | Art Unit | |
| | Horace L. Flournoy | 2189 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *21 July 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-12* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-12* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *21 July 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☒ Certified copies of the priority documents have been received in Application No. 10/623,916.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

## DETAILED ACTION

Claims 1-12 are presented for examination.

### *Priority*

Acknowledgment is made of applicant's claim for foreign priority under 35 U.S.C. 119(a)-(d). The certified copy has been filed in parent Application No. 02405643.4, filed on 7/23/2002.

### *Claim Rejections - 35 USC § 102*

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1, 2, 6, 8-12 are rejected under 35 U.S.C. 102(b) as being anticipated by Durig et al. (U.S. Patent no. 6,084,849 hereafter referred to as Durig).

With respect to independent claim 1,

"A data processing system comprising: a local probe storage array having a plurality of sensors for reading data from a storage surface;" is disclosed in column 1, lines 40-49.

The examiner interprets the limitation "sensors for reading data" as analogous to read/write heads.

Durig discloses in column 6, lines 4-12, "A scanning probe storage system in accordance with the present invention, further comprises local probe array with cantilevers 52.1-52.4, as illustrated in FIG. 7. Each cantilever carries at least one tip for interaction with the storage fields 54.1-54.4 of the storage medium. The array of cantilevers with the respective tips is scanned as a whole over the corresponding storage fields 54.1-54.4 and the data in each storage field are addressed quasi-simultaneously."

Durig teaches a local probe storage array having a plurality of sensors (A scanning probe storage system in accordance with the present invention, further comprises local probe array with cantilevers) for reading data (scanning data) from a storage surface (storage fields 54.1-54.4 of the storage medium).

Durig further discloses in column 1, lines 40-49, "Opposite to these cantilevers there are hundreds of read/write heads which are similar in nature to scanning tunneling or atomic force microscope scanning tips. Each cantilever is moved in an oscillatory manner such that the respective read/write head scans over the bits stored thereon." (U.S. Pat. No. 5,307,311, incorporated by reference by Durig and hereafter referred to as Sliwa).

Sliwa teaches a plurality of sensors (read/write heads next to the cantilevers).

"...a plurality of data processing elements mounted on the storage array and each connected to different sensor of the array for processing data read by said connected sensor" is disclosed in Sliwa in column 4, lines 35-67.

The examiner interprets the limitation "data processing elements" as logic elements or components of a processor.

Sliwa discloses in column 2, lines 6-11, "The cantilevers are given their oscillatory motions in one of several possible ways, including driving by a coupled piezoelectric or electrostrictive resonator, by Coulomb forces created across capacitively-coupled electrodes (one of which resides on each moving cantilever)..."

Sliwa teaches a data processing element (capacitively-coupled electrode) each connected to a different sensor (cantilever).

With respect to claim 2 and independent claims 11 and 12,

"A data processing system as claimed in claim 1, wherein the storage surface comprises a plurality of data fields each corresponding to different one of the sensors and each having a matrix of bit storage locations individually addressable by the corresponding sensor" is disclosed in Durig column 1, lines 43-44, column 6, lines 4-12 and also in Sliwa column 1, lines 67-68, column 2, lines 22-25.

Durig discloses in column 1, lines 43-44 "It employs an array of hundreds of microcantilevers having an area in which bits are stored."

Sliwa recites in column 1, lines 67-68 and column 2, lines 22-25, "Each cantilever has disposed on its surface an array of storage bits called a bit array. Opposite the bit array surface region of each cantilever is a read/write head...Choices exist for placing either the bit-array(s) or the read/write head on the moving cantilever with its counterpart being disposed on the remaining opposite surface. Further choices exist involving the cantilever shape and direction of driving such that both linear and two dimensional bit arrays can be utilized and physically addressed."

Sliwa teaches a storage surface (storage bits) that comprises a plurality of data fields (bit-array) each corresponding to different one of the sensors and each having a matrix (array) of bit storage locations individually addressable (physically addressed) by the corresponding sensor.

With respect to claim 6 and independent claims 11 and 12,

"A data processing system œs claimed in claim 3, wherein each field of the storage surface has different bit locations assigned to different memory pages." is disclosed in column 2, lines 58-62.

The examiner interprets the limitation "memory pages" as memory locations or physical storage addresses.

Sliwa discloses in column 21, lines 58-62, "If the areal arrays are to be physically addressed, one requires relative areal scanning motion of the bit array relative to the read/write head which is dedicated to that bit array."

Sliwa teaches each field of the storage surface has different bit locations assigned to different memory pages (read/write head which is dedicated to that bit array).

With respect to claim 8,

"A data processing system as claimed in claim 1, wherein the data processing elements comprise logic for comparing an input bit pattern with a bit pattern recorded on the storage surface." is disclosed in column 11, lines 15-24.

Sliwa discloses in column 11, lines 15-24, "One may choose to utilize one or more cantilever devices to read a spatial reference pattern of positional data written on its bit-array, thus providing a signal which is a function of unwanted displacement and acceleration to the corrective means which may, as described, consist of corrective damping or cancellation resonator motions. The same reference pattern may aid in tip position determination on all cantilevers, as is done with tracks and sectors on magnetic disk drives.

Sliwa teaches data processing elements comprise logic for comparing an input bit pattern (in tip position determination on all cantilevers) with a bit pattern recorded on the storage surface (spatial reference pattern of positional data written on its bit-array).

With respect to claim 9,

"A data processing as claimed in claim 1, wherein at least one of the data processing elements comprises a microprocessor" is disclosed in the abstract.

The examiner interprets the limitation "data processing elements" as logic elements or components of a processor.

Sliwa discloses in the abstract, "Electronic support circuitry is provided to implement the memory device of the invention. Such circuitry includes a microprocessor (67), a multiplexer/demultiplexer (70), a group of circuits (66) comprising power supplies, sensing circuits and digital/analog and analog/digital conversion circuits, and switching means (65) to permit all of the previous functions to be properly addressed to/from the correct bit/array(s) and mating subdevice(s)."

With respect to independent claim 10,

"A data processing method comprising: reading data from a storage surface via sensors of a local probe storage array..." is disclosed in column 6, lines 4-12.

Durig discloses in column 6, lines 4-12, "A scanning probe storage system in accordance with the present invention, further comprises local probe array with cantilevers 52.1-52.4, as illustrated in FIG. 7. Each cantilever carries at least one tip for interaction with the storage fields 54.1-54.4 of the storage medium. The array of

cantilevers with the respective tips is scanned as a whole over the corresponding storage fields 54.1-54.4 and the data in each storage field are addressed quasi-simultaneously."

"...and processing the data read from the surface via a plurality of data processing elements mounted on the storage array and each connected to a corresponding one of the sensors of the array" is disclosed in column 2, lines 6-11.

Sliwa discloses in column 2, lines 6-11, "The cantilevers are given their oscillatory motions in one of several possible ways, including driving by a coupled piezoelectric or electrostrictive resonator, by Coulomb forces created across capacitively-coupled electrodes (one of which resides on each moving cantilever)..."

Sliwa teaches a data processing element (capacitively-coupled electrode) each connected to a different sensor (cantilever).

With respect to independent claim 11,

"A memory for storing data comprising a local probe storage array having a plurality of sensors for reading data from a storage surface,

Durig discloses in column 6, lines 4-12, "A scanning probe storage system in accordance with the present invention, further comprises local probe array with cantilevers 52.1-52.4, as illustrated in FIG. 7. Each cantilever carries at least one tip for interaction with the storage fields 54.1-54.4 of the storage medium. The array of

cantilevers with the respective tips is scanned as a whole over the corresponding storage fields 54.1-54.4 and the data in each storage field are addressed quasi-simultaneously."

"...the storage surface comprising a plurality of data fields each corresponding to different one of the sensors and each having a matrix of bit storage locations individually addressable by the corresponding sensor," is disclosed as stated supra.

"...wherein each field of the storage surface has different bit locations assigned to different memory pages." is disclosed as stated supra.

With respect to independent claim 12,

"A method for storing data in a local probe storage array having a plurality of sensors for reading data from a storage surface,

Durig discloses in column 6, lines 4-12, "A scanning probe storage system in accordance with the present invention, further comprises local probe array with cantilevers 52.1-52.4, as illustrated in FIG. 7. Each cantilever carries at least one tip for interaction with the storage fields 54.1-54.4 of the storage medium. The array of cantilevers with the respective tips is scanned as a whole over the corresponding

storage fields 54.1-54.4 and the data in each storage field are addressed quasi-simultaneously."

"...the storage surface comprising a plurality of data fields each corresponding to different one of the sensors and each having a matrix of bit storage locations individually addressable by the corresponding sensor," is disclosed as stated supra.

"...the method comprising assigning different bit locations of each field of the storage surface to different memory pages" is disclosed as stated supra.

***Claim Rejections - 35 USC § 103***

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham v. John Deere* CO., 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

Claim 3 is rejected under 35 U.S.C. 103(a) as being obvious over Durig (U.S. Patent no. 6,084,849) in view of Shum et al. (US Patent No. 6,865,645 hereafter referred to as Shum).

With respect to claim 3, Durig teaches "A data processing system as claimed in claim 2..." as stated supra.

Durig, however, does not disclose expressly "...wherein the storage surface comprises a user data portion dedicated to storage of user data for manipulation by the processing elements, and a program code portion dedicated to storage of program code for configuring the processing elements to manipulate the user data."

Shum discloses in column 2 lines 26-29, 43-54, "The FIGURE depicts a multi-processor system 10 including separate instruction cache (I-cache) and Data or Operand cache (D-cache)...As a consequence, whenever a particular central processing unit 100 attempts to write to a memory location, it must first inform all other central processing units 100 of its desire to write to the location and receive permission from all other processing elements to carry out the write." Shum teaches in the FIGURE the memory area (storage surface) which has a portion of section of its memory or surface that stores user data (data cache) and a portion or section that stores program

code (instruction cache) for manipulation and configuring of processing elements (permission to carry out the write/read).

Durig and Shum are analogous art because they are from the same field of endeavor, that being devices for processing data.

At the time of the invention it would have been obvious to a person of ordinary skill in the art to combine a storage surface with user data portion and a program code portion each for manipulation by processing elements with the data processing system of claim 1.

The motivation for doing so would have been obvious based on the teaching of Shum in column 1, lines 48-61, "In a multiprocessor computer system, it is important to provide a coherent memory system, that is, to cause writes to each individual memory location to be serialized in some order for all central processing units...A multiprocessor system that implements these properties is said to be "coherent." Shum further teaches in column 2 lines, 4-13, "The cache coherency protocol allows shared access by the instruction cache and the operand cache to a cache block if it has read only status. In addition, the cache coherency protocol allows access by the operand cache and prevents access by the instruction cache to a cache block if it has exclusive status...The cache coherency protocol includes interfaces with a multi-processor system storage controller employing a multi-processor cache coherency protocol as well as interfaces with existing cache handling requirements."

Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention having the teachings of Durig and Shum before him/her to combine

Shum and Durig for the benefit of combining a storage surface with user data portion and a program code portion each for manipulation by processing elements with the data processing system of claim 1 to obtain the invention as specified in Claim 3.

Claim 4 is rejected under 35 U.S.C. 103(a) as being obvious over Durig (U.S. Patent no. 6,084,849) in view of Shum et al. (US Patent No. 6,865,645 hereafter referred to as Shum).

With respect to claim 4, Durig teaches "A data processing system as claimed in claim 3..." as stated supra.

Durig, however, does not disclose expressly "...wherein the program code portion and the user data portion are located in different fields of the storage surface."

Shum discloses in column 2 lines 26-29, 43-54, "The FIGURE depicts a multi-processor system 10 including separate instruction cache (I-cache) and Data or Operand cache (D-cache)...As a consequence, whenever a particular central processing unit 100 attempts to write to a memory location, it must first inform all other central processing units 100 of its desire to write to the location and receive permission from all other processing elements to carry out the write." Shum teaches in the FIGURE the memory area (storage surface) which has a portion of section of its memory or surface that stores user data (data cache) and a portion or section that stores program code (instruction cache) for manipulation and configuring of processing elements (permission to carry out the write/read).

Durig and Shum are analogous art because they are from the same field of endeavor, that being devices for processing data.

At the time of the invention it would have been obvious to a person of ordinary skill in the art to combine a program code portion and a user data portion located in different fields of the storage surface with the data processing system of claim 3.

The motivation for doing so would have been obvious based on the teaching of Shum in column 1, lines 48-61, "In a multiprocessor computer system, it is important to provide a coherent memory system, that is, to cause writes to each individual memory location to be serialized in some order for all central processing units...A multiprocessor system that implements these properties is said to be "coherent." Shum further teaches in column 2 lines, 4-13, "The cache coherency protocol allows shared access by the instruction cache and the operand cache to a cache block if it has read only status. In addition, the cache coherency protocol allows access by the operand cache and prevents access by the instruction cache to a cache block if it has exclusive status...The cache coherency protocol includes interfaces with a multi-processor system storage controller employing a multi-processor cache coherency protocol as well as interfaces with existing cache handling requirements."

Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention having the teachings of Durig and Shum before him/her to combine Shum and Durig for the benefit of combining a program code portion and a user data portion located in different fields of the storage surface with the data processing system of claim 3 to obtain the invention as specified in Claim 4.

Claim 5 is rejected under 35 U.S.C. 103(a) as being obvious over Durig (U.S. Patent no. 6,084,849) in view of Shum et al. (US Patent No. 6,865,645 hereafter referred to as Shum).

With respect to claim 5, Durig teaches "A data processing system as claimed in claim 3..." as stated supra. Sliwa teaches field of at least one bit (bit array) in column 1, lines 67-68.

Durig, however, does not disclose expressly "...wherein each field of the storage surface has at least one bit location assigned to the program code portion and at least one bit location assigned to the user data portion."

Shum discloses in column 2 lines 26-29, 43-54, "The FIGURE depicts a multi-processor system 10 including separate instruction cache (I-cache) and Data or Operand cache (D-cache)...As a consequence, whenever a particular central processing unit 100 attempts to write to a memory location, it must first inform all other central processing units 100 of its desire to write to the location and receive permission from all other processing elements to carry out the write." Shum teaches in the FIGURE the memory area (storage surface) which has a portion of section of its memory or surface that stores user data (data cache) and a portion or section that stores program code (instruction cache) for manipulation and configuring of processing elements (permission to carry out the write/read).

Durig and Shum are analogous art because they are from the same field of endeavor, that being devices for processing data.

At the time of the invention it would have been obvious to a person of ordinary skill in the art to combine a feature of each field having at least one bit with the data processing system of claim 3.

The motivation for doing so would have been obvious based on the teaching of Shum in column 1, lines 48-61, "In a multiprocessor computer system, it is important to provide a coherent memory system, that is, to cause writes to each individual memory location to be serialized in some order for all central processing units...A multiprocessor system that implements these properties is said to be "coherent." Shum further teaches in column 2 lines, 4-13, "The cache coherency protocol allows shared access by the instruction cache and the operand cache to a cache block if it has read only status. In addition, the cache coherency protocol allows access by the operand cache and prevents access by the instruction cache to a cache block if it has exclusive status...The cache coherency protocol includes interfaces with a multi-processor system storage controller employing a multi-processor cache coherency protocol as well as interfaces with existing cache handling requirements."

Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention having the teachings of Durig and Shum before him/her to combine Shum and Durig for the benefit of combine a feature of each field having at least one bit with the data processing system of claim 3 to obtain the invention as specified in claim 5.

Claim 7 is rejected under 35 U.S.C. 103(a) as being obvious over Durig (U.S. Patent no. 6,084,849) in view of Batcher (US Patent No. 4,314,349 hereafter referred to as Batcher).

With respect to claim 7, Durig teaches "A data processing system as claimed in claim 1..." as stated supra.

Durig, however, does not disclose expressly "...further comprising a random access memory mounted on and connected to the data processing elements."

Batcher discloses in column 1 lines 65-69 and column 2 lines 1-3, " Further, it is desirable that each processing element be capable of performing all of the Boolean operations possible between two bits of data, and that each such processing element include its own random access memory. Yet further, for such a system to be efficient, it should include means for bypassing inoperative or malfunctioning processing elements without diminishing system integrity."

Durig and Batcher are analogous art because they are from the same field of endeavor, that being devices for processing data.

At the time of the invention it would have been obvious to a person of ordinary skill in the art to combine a RAM(s) mounted on and connected to the data processing elements of the local probe storage array of claim 1.

The motivation for doing so would have been obvious based on the teaching of Sliwa (incorporated by reference by Durig) in column 1, lines 21-33, "On the other hand,

solid state memories such as DRAM (dynamic random access memory), SRAMs (static RAM) and EEPROMs (electrically erasable programmable nonvolatile memory) offer much higher read/write speeds on the order of nanoseconds...Of great value would be a memory device combining the capacity of rotating memory with the speed, size, and reliability of solid state memory. With it, computers would take another quantum leap in performance and compactness as well as in reliability."

Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention having the teachings of Sliwa and Batcher before him/her to combine Batcher and Sliwa for the benefit of having speed and efficiency enhancements of RAM(s) mounted on and connected to the data processing elements of the local probe storage array of claim 1 to obtain the invention as specified in Claim 7.

## ***Conclusion***

Any inquiry concerning this communication or earlier communication from the examiner should be directed to Horace L. Flournoy whose telephone number is (571) 272-2705. The examiner can normally be reached on Monday-Friday 7:00 AM to 4:30 PM (ET).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Don Sparks can be reached on (571) 272-4201. The fax phone numbers for the organization where this application or proceeding is assigned is (703) 746-7239

Information regarding the status of an Application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or PUBLIC PAIR. Status information for unpublished applications is available through Private Pair only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (571) 272-2100.

Horace L. Flournoy
Patent Examiner
Art unit: 2189

CHRISTIAN CHACE
PRIMARY EXAMINER
Primary Patent Examiner
Technology Center 2100